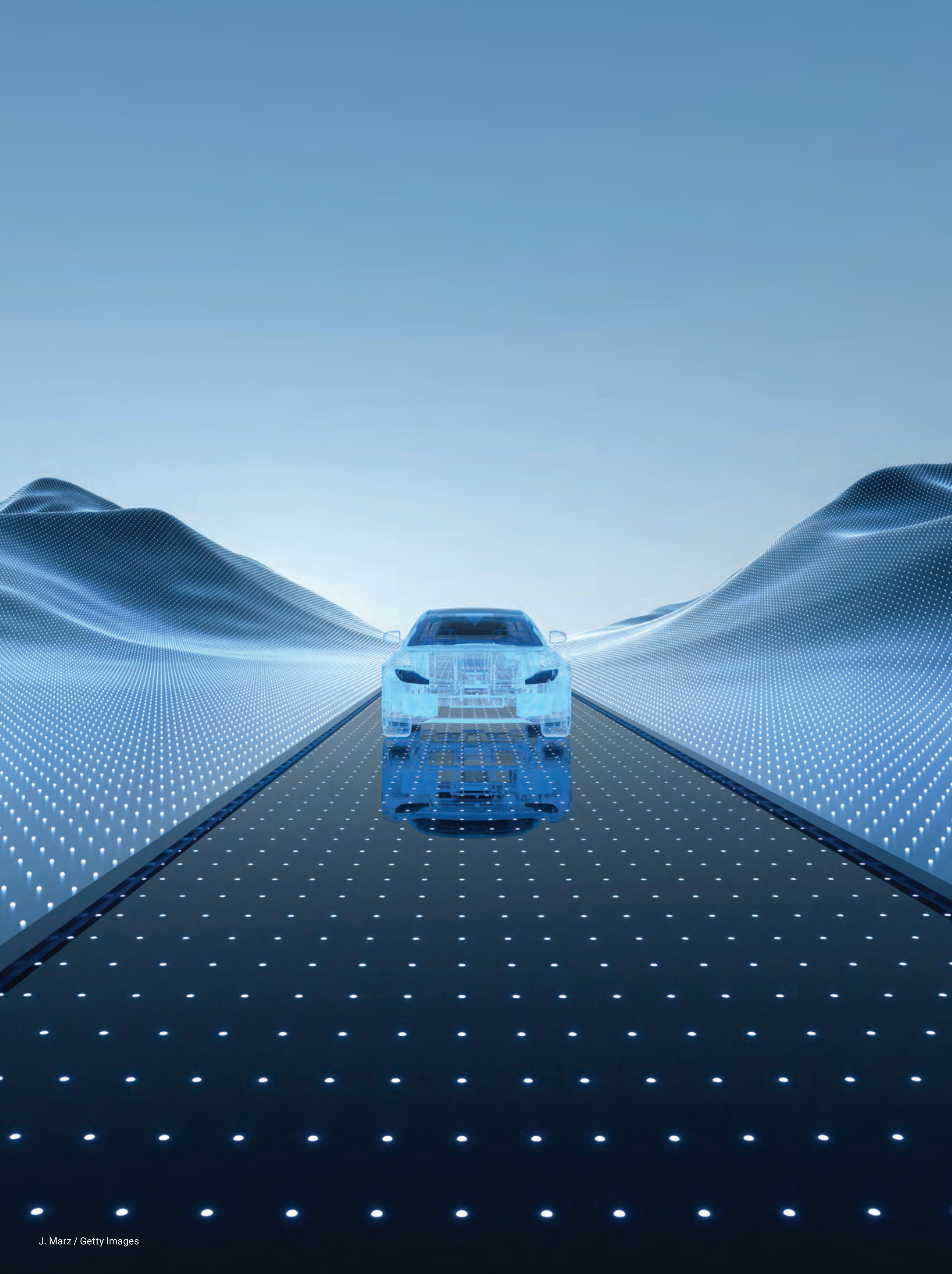

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Photonics for Processing

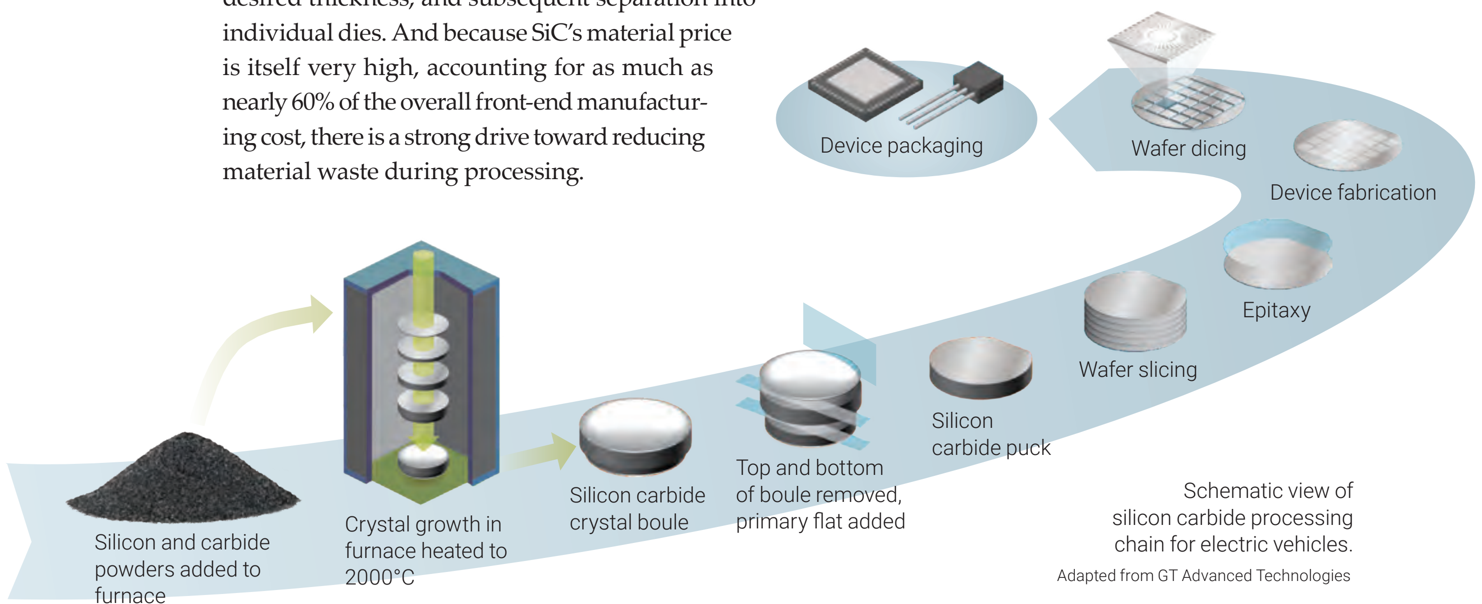
Wide-Bandgap Semiconductors

Benjamin Bernard

Lasers and advanced optics are key enablers for processing the emerging materials that underpin EVs, power electronics, smart grids and the electrification of society.

The move toward decarbonization and electrification of much of daily life puts semiconductor development in the spotlight. The quest for power devices with improved electrical performance has particularly raised interest in new materials like silicon carbide (SiC) and gallium nitride (GaN), often referred to as wide-bandgap (WBG) semiconductors.

But while SiC in particular brings some unique advantages to the table for electric vehicles (EVs) and other power electronics, manufacturing this material also carries some special challenges. For one thing, SiC has a hardness of 9.5 on the Mohs scale—very close to that of diamond—which complicates the machining of the wafers, such as grinding to achieve the desired thickness, and subsequent separation into individual dies. And because SiC's material price is itself very high, accounting for as much as nearly 60% of the overall front-end manufacturing cost, there is a strong drive toward reducing material waste during processing.



Schematic view of silicon carbide processing chain for electric vehicles.

Adapted from GT Advanced Technologies

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Photonics already plays a major role within the semiconductor manufacturing chain, and has demonstrably aided and in some cases even enabled certain key processing steps. This article offers a deeper look at how collimated light adds value in WBG semiconductor manufacturing in supply chains for emerging technologies such as EVs. After a brief introduction to WBG materials, we will look at how advanced optics and state-of-the-art laser systems play a key role at various steps, from splitting and slicing the crystal boule into individual wafers through subsequent front-end processes (those at the wafer level) and back-end fabrication steps (such as wafer dicing and device packaging).

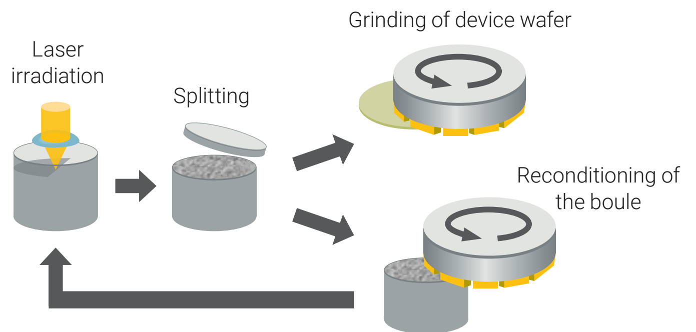
Why WBG?

WBG semiconductors can be uniquely advantageous for electric vehicles (EVs) and other power electronics, because breakdown voltage—the value at which parts of the insulator become electrically conductive—is directly linked to the band gap. The band gaps of SiC (3.2 eV) and GaN (3.4 eV) are each around three times higher than that of silicon (1.1 eV). This converts to roughly an order-of-magnitude-higher breakdown voltage for WBG materials versus silicon for material of comparable thickness and doping level. That difference, in turn, leads to improved efficiency, higher operating voltages, faster switching speeds and reduced system footprint (due to improved heat dissipation) compared with classical silicon-based devices.

Does this mean that WBG semiconductors might someday completely replace silicon? Hardly. For applications requiring blocking voltages below 600 V—including most consumer electronics—silicon technology will remain the principal contributor; indeed, silicon supply chains have been better optimized for reliable mass production than for perhaps any other product in history.

If voltages higher than 600 V or fast switching are needed, however, WBG materials start to gain favor—and companies become willing to go the extra mile to set up production lines to fabricate only GaN- and SiC-based devices. Typical applications for WBG materials include high-speed railways, power transmission, industrial drives, smart grids and wind power generation.

While both GaN and SiC are attracting increasing interest, GaN still underperforms theoretically achievable breakdown voltage levels. That's because pure GaN is very hard to handle and bring to commercial yields. Almost all commercially available GaN devices use a silicon or sapphire substrate as support, with a GaN layer around 5 μm or less in thickness epitaxially grown on top. Mismatches between materials at the interface and additional impurities in the GaN stack itself tend to reduce the actually realized breakdown voltage.



A schematic view of boule-splitting shows the creation of a 350-m-thick wafer from a 20-mm-thick SiC boule using KABRA, a laser-based process developed by Disco Corp., Tokyo, Japan. The laser modifies the boule at a specific depth, and the wafer is mechanically split from the bulk material. The surfaces of both the wafer and the remaining bulk material are conditioned by grinding, and the bulk material is returned for creation of another wafer.
Adapted from original by Disco Corp.

In light of this, most of the discussion below focuses on lasers and optics in SiC processing—though we do cover the important step of laser grooving and separation of GaN devices grown on silicon substrates. (For more on SiC, see "Silicon Carbide: From Abrasives to Quantum Photonics," OPN, March 2021, p. 34.)

Boule splitting

SiC processing begins with crystal growth in a furnace to obtain a crystal boule, subsequently shaped into the SiC "puck," to be sliced into individual wafers. Because of SiC's high material cost, there's a strong incentive to increase the yield of available wafers from one boule. The classic abrasive method—slicing the boule into individual wafers using a diamond saw—sacrifices a significant amount of material (around 180 μm thickness), and also seems to impose a lower limit of around 350 μm thickness for the resulting sliced wafer. That's mainly because of the high amount of mechanical stress introduced by the wire saw and the risk of breakage when the thin wafer is released.

Photonics-based processes have helped to overcome these issues. In these methods, a laser is focused inside the SiC boule to create a modification area that weakens the material at a defined depth; when an external stress is applied, the wafer can be split from the bulk.

Eunho Kim and colleagues at the University of Kyoto, Japan, for example, demonstrated the slicing of a 420-μm-thick 4H–SiC wafer using a 780-nm

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femtosecond laser in a double-pulse configuration. To compensate for the spherical aberration introduced by SiC's high refractive index at that wavelength ($n = 2.6$), the team used a spatial light modulator and scanned line by line, with a constant hatch of 25 μm at a depth of around 260 μm inside the wafer. After tensile stress was applied using a universal testing machine, the wafer was split in two parts, with a measured surface roughness of 5 to 24 μm—significantly lower than is possible with a diamond saw. High-volume laser-based boule splitting has already found its way into industry and is commercially available.

Lithography

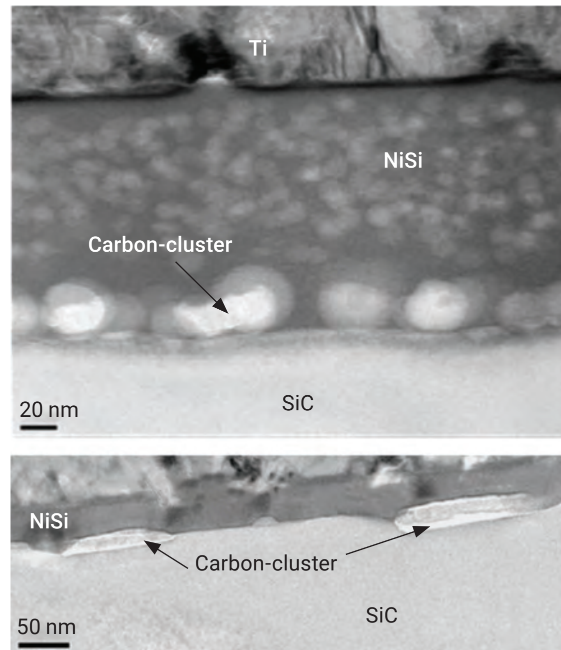
Lithography, the printing technology for producing a 3D-relief image on a substrate, is the key enabler of chip mass production. The general sequence of steps is substrate preparation, photoresist spin coating, exposure and development; the sequence is run several times in a loop until the final device architecture is realized.

The heart of the lithography process is imaging the photomask onto the wafer. The mask contains the structure to be printed on the wafer as opaque patterns on a transparent substrate, to partially expose areas of the resist. After use of a wet-chemical developer, the exposed areas are removed and the patterned resist layer remains. The minimum feature sizes, often referred to as the critical dimension (CD), are directly linked to the wavelength of the light and the numerical aperture (NA) of the optics.

Deep-ultraviolet (DUV) excimer lasers are now commonly used to reach wavelengths of 248 nm (KrF) and 193 nm (ArF) in lithography systems. Further reducing the wavelength adds additional complexity to the system architecture due to strong absorption by air of light below 193 nm. For many power device applications, the DUV laser sources mentioned above, combined with sophisticated optical systems, are good enough to reach the targeted feature sizes, but for the latest microcontrollers there is already a drive to go toward 3 nm.

Back-side contact annealing

For many applications, "less is more" is the watchword for final device thickness. The "on-resistance," for



Transmission electron micrograph of the back-side metal stack annealed NiSi layer, created with laser thermal annealing (top) and classical furnace annealing (bottom). Laser thermal annealing leads to much smaller carbon clusters.

Reprinted with permission from R. Rupp et al., 25th Intl. Sympos. Power Semicond. Dev. ICs, Kanazawa, Japan, 51-54 (2013); © 2013 IEEE

example—the value of resistance between drain and source of relay during operation—is directly linked to the thickness of the device. Further, the heat flux through the device, the nondestructive surge current density and the device's general reliability benefit from thin wafer technologies.

While all of this is attractive from a design point of view, achieving minimum device thickness adds challenges and complexity to the manufacturing process. Each process step after the grinding (thinning down the wafer to the target thickness) risks wafer breakage, so the aim is to reduce those steps as much as possible. For SiC, the situation is even more critical than for silicon, due to the high thermal load (1000°C) needed for the ohmic contact formation on the back side, where the wafer of course must already be in a thinned state. Classical furnace processes don't allow completion of front-side Schottky metallization (with metals such as

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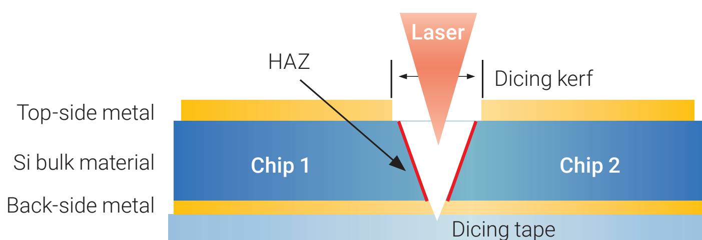
titanium, tungsten and nickel) before back-side contact formation. Schottky metals tend to form silicides with SiC at temperatures greater than 500°C, which can block the Schottky interface.

Laser thermal annealing is an optimal solution to overcome this problem. The laser beam's precise, localized energy distribution allows formation of ohmic contacts on the back side without heating up the front side, and therefore offers the possibility of fully manufacturing the front side before back-side grinding.

Apart from this simplification of the process flow, laser thermal annealing also improves the structure of the ohmic contact itself, by eliminating the development of large carbon clusters. These can weaken the stability of the back-side metallization interface and lead to exfoliation at further process steps or, in the worst case, during operation in the product's final use. R. Rupp and colleagues, from Infineon Technologies, investigated this phenomenon in detail by applying 150-ns, 310-nm-wavelength laser pulses with a 15×15-mm spot size in a step-and-repeat scan of the whole back-side metallization of a wafer, with an overlap of around 10% between individual shots. Compared with a furnace process, the laser-based approach led to a significant difference in the formation of carbon clusters.

Separation

Dicing, the separation of the wafer into individual dies, is a crucial process step. While it adds no value to the wafer itself, dicing is directly linked to the incoming back-end yield. High mechanical robustness of the chip after separation is important to hold up to subsequent process steps like pickup from the transportation foil, soldering into the package, wire bonding to be connected to the rest of the world and the heating-up of the device under actual operating conditions.



Cross-section of a wafer diced by laser ablation. A heat-affected zone (HAZ) is created during laser processing that affects the mechanical robustness of the chip.

Several laser-based separation strategies are in use, all with pros and cons. Non-ablative dicing, where a laser pulse is focused inside the material to create a modification line along the cutting direction, is generally fast and mechanically robust, due to the defined small interaction zone. The downside is that this technique requires an additional process step (tap expansion, mechanical breaking or thermal stress) to introduce tensile stress along the line of laser-induced modification.

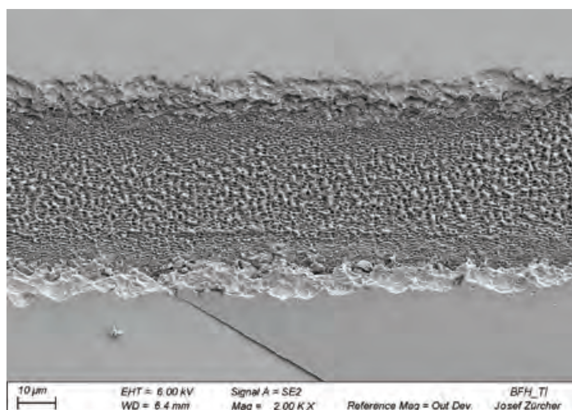
Non-ablative dicing also requires that the dicing kerf—the dedicated space on the wafer surrounding each chip to be separated—to be transparent, so the laser can focus inside. Usually process control monitoring structures made of metals are placed inside dicing kerfs to measure the electrical performance without sacrificing active area for chips. For SiC, with its high material cost, the issue is even more critical, and transparent kerf is mostly unavailable.

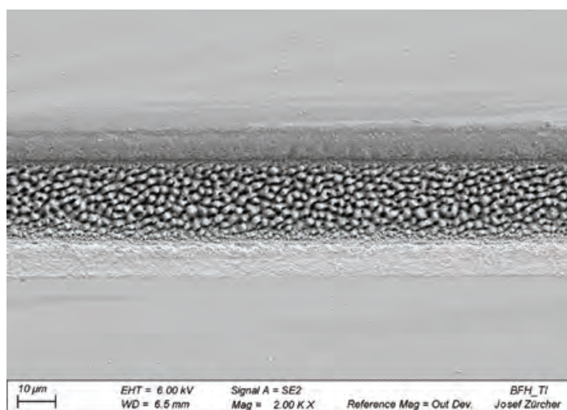
Ablative laser dicing, in which the focus is placed on the surface and material is removed until the wafer is separated, is more suitable for kerfs with metals because it doesn't require a transparent kerf and can remove any material. Since it's a thermally driven process, however, a certain damage zone is introduced into the remaining sidewall of the chip. This heat-affected zone (HAZ) reduces mechanical integrity and can be manipulated in size by laser processing conditions. In general, the higher the throughput of the cut, the larger the HAZ. But recent approaches using beam shaping or beam splitting by diffractive optical elements have achieved improvements in both speed and cut quality.

Grooving

As already noted, the situation is slightly different for GaN, which is epitaxially grown as a very thin layer on silicon or sapphire. Thus very gentle laser processing is required.

Since power GaN devices are mainly grown on a silicon substrate, the separation is based on a hybrid process that includes laser grooving of the GaN followed





Comparison of a GaN layer grooved using lasers of wavelengths 1030 nm (left) and 343 nm (right). UV laser radiation leads to defined grooving edges, without the chipping that results with IR grooving. Courtesy of B. Neuenschwander

by blade dicing of the remaining silicon. Usually, the silicon thickness is 200 to 300 µm, and not so attractive in terms of throughput to be cut by the laser. Mechanical separation of the GaN from the silicon, on the other hand, is very challenging due to the risk of delamination or peel-off from the bulk substrate; moreover, GaN tends to contaminate the blade, leading to clogging and a reduced cut quality.

Beat Neuenschwander from the Bern University of Applied Sciences, Switzerland, compared picosecond and femtosecond laser pulses at IR, visible green and UV wavelengths for the removal of a 5-µm GaN layer on a silicon substrate. He found that using IR easily leads to chipping along the grooving traces and the presence of less-defined grooving edges. It seems that the reduced optical penetration depth of shorter wavelengths is beneficial and allows more stable process conditions.

The laser grooving step is the main contributor to the chip's mechanical robustness after the chip is finally separated by the blade cut. The recent switch toward ultrashort-pulse lasers for laser grooving, compared with the nanosecond pulses previously used, has significantly improved chip robustness. To ensure a complete removal of the GaN stack and have a stable process window, a certain amount of the silicon substrate needs to be ablated as well. Short-pulse processing is also increasing quality by reducing the size of the HAZ.

Lift-off

GaN-based light-emitting diodes (LEDs) are usually grown on sapphire substrates, which offer a smaller interface mismatch and, thus, a higher quality in the epitaxially grown GaN than silicon substrates. However, sapphire's poor electrical and thermal conductivity can have a negative effect on final LED performance. The solution is to strip the GaN from the sapphire substrate by laser lift-off (LLO), transferring it via wafer bonding to a substrate with better conductivity for the final application. This approach is also used to fabricate 2D or 3D microstructures.

During LLO, the laser is focused through the sapphire on the strongly absorbing interface layer (often a polymer) that holds both stacks together. When the interface layer is evaporated by the laser, the GaN can lift off and be released from the bulk material. To avoid damaging the functional GaN layer, UV excimer lasers at 248 nm, which allow a defined, precise ablation of the interface, are the tool of choice.

Lasers everywhere

Aside from the laser applications highlighted above, lasers show up at a range of other points in the WBG semiconductor processing chain. Laser marking is used to place an ID code on the wafer, for example. Lasers also factor into chip trimming, to selectively open certain contacts to manipulate the electrical performance. And low-power laser systems are used to inspect the wafer as it proceeds through a variety of different processing steps.

As this brief survey suggests, lasers and optics have been, and remain, key enabling technologies for the WBG semiconductors that could play a central role in a cleaner, electrified future. Continual improvement in laser systems and new optical concepts will further improve the semiconductor manufacturing chain—pointing to a bright future for photonics in this area. OPN

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For references and resources, go online: optica-opn.org/link/0524-wbgs.

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